R&D facilities at ECE Department:

Established in 2010, our **VLSI & Embedded System Research Laboratory** has been advancing through research in various fields of electronics engineering, and providing knowledge by delivering information to the students. The researchprojects carried out in this laboratory is focused on a wide area of research in the fields of VLSI, reconfigurable computing and embedded technology. Some significant design projects have been published in various journals and conferences. A brief account is given below:

Infrastructure / Facilities available:

EDA tools for VLSI design :

1. **Cadence (2010-2014):**
   Cadence VLSI tool consisting of Analog/Digital front-end and backend and High speed PCB Design tool.
   - Virtuoso(R) Analog Design Environment
   - Virtuoso(R) Schematic VHDL Interface
   - Virtuoso(R) Schematic Editor Verilog(R) Interface
   - Assura(TM) Layout Vs. Schematic Verifier
   - Allegro PCB Design XL.
   - Spectre Circuit Simulator

2. **Mentor Graphics IC Nanometer Design Bundle Tools (HEP-1) (2014-present)**

   The tool provides a complete environment for the VLSI design, capture, layout and verification of analog, digital and mixed-signal integrated circuits. The tool includes,

   The Pyxis suite of IC design tools
   - Schematic capture, netlisting, simulation set-up and results viewing.
   - Physical layout
   - Editing, schematic-driven layout, and top-level floor planning and routing.

   Questa ADMS and Questa AMDS RF - A language-neutral, mixed-signal simulator that enables top-down design and bottom-up verification of multi-million gate analog/mixed-signal SoC designs.

   Eldo and Eldo RF - An analog simulator offering numerous simulation and modelling options that deliver high-performance and high-speed simulation with the accuracy required by the user.

   ADiT™ - A fast-SPICE simulator built specifically for analog and mixed signal applications.

Calibre - The industry standard platform for physical verificationand design for manufacturability of deep sub micron integrated circuits, offering superior performance and capacity for both flat and hierarchical algorithms.

Calibre xRC- Accurate transistor-level, gate-level and hierarchical parasitic extraction.

Tools for Embedded system and Reconfigurable computing

3. **XILINX Integrated Synthesis Environmentfor synthesis and analysis of HDL designs**
    - ISE foundation
    - Chip scope pro
4. **Xilinx FPGA products**
    - Spartan 3AN Starter kit
    - Virtex 5ML 501 evaluation and development board

5. **pSOC boards(From Cypress Inc):**

As the name suggests, this can be used to design one's own SOC programmatically, we are researching on using this in designing a "Lab-on-a-chip", where students can configure it to setup any laboratory experiment in the field of "Electronics and Communication".

6. **ARM 7 platform**
    - ARM-7 LPC2148
    - IDE for ARM 7
    - RFID kit
    - Touch screen interfacing kit
    - GSM modem interfacing kit
    - Graphic LCD interfacing kit

Signal Processing and Embedded design:

7. **MATLAB**

    - MATLAB
    - Simulink
    - Real time workshop
    - Target support package
    - Embedded IDE link
    - Real time workshop embedded coder
    - Signal processing toolbox
    - Signal processing block set
    - Communication tool box
    - Communication block set
    - Fixed point toolbox

- Simulink fixed point
- Matlab report generator
- Control system toolbox

8. **Digital Signal Processing**
    - Texas TMS320C6713 development kit.
    - Code composer studio IDE

Major research work carried out in this laboratory

- Low power combinational circuit design using Cyclic Combinational Gate Diffusion Input Technique:
- Low power High Speed CMOS OP-AMP design
- High Speed ALU design using full swing TG
- Low power high speed ring modulator based VCO design
- Design & study of low power high speed full adder circuits.
- Sequential & combinational circuit design using ternary logic
- Reconfigurable modulator based on Ternary Logic
- Configurable modulator design using ternary logic
- Design & study of low power high speed Look ahead Carry generator
- Compressed Sensing Image Reconstruction using Multichannel Fusion and Adaptive Filtering
- GDI dual edge triggered DFF design
- Low power Vedic multiplier design using GDI
- Adiabatic logic for low power and low noise systems.
- Hybridization of adiabatic logic and CMOS logic.
- Adiabatic logic for reversible computing.
- A true "Lab-on-a-chip"
- Processor with reconfigurable DSP system

Training program carried out

1) Winter workshop on VLSI & Embedded System Design, a training program carried out in this lab during January 2014.
2) Summer workshop on
    (i)Embedded System Design Using Microcontrollers and FPGA
    (ii)Processor Architecture and System-on-Chip Design
    Duration: (25.06.14-11.07.14)